IN THE CLAIMS:

Please cancel claims 2, 3, 12, and 13 without prejudice.

Please amend claims 1, 4, 11, 14, and 20 as indicated in attached Appendix A.

A listing of the status of all claims 1-20 in the present patent application is provided in attached Appendix A.

APPENDIX A

1 (Currently Amended). A method for synchronizing clocks in a network, the method comprising the steps of:

receiving a first timestamp and a second timestamp each indicating a respective time instance within the network;

delaying the first timestamp by a first delay amount;

measuring a first time interval between the first timestamp delayed by the first delay amount and the second timestamp as determined by a first clock signal;

delaying the first timestamp by a second delay amount;

measuring a second time interval between the first timestamp delayed by the second delay amount and the second timestamp as determined by a second clock signal;

generating a difference signal representing a difference between the first time interval and the second time interval;

filtering the difference signal; and

generating the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal.

2 (Cancelled). The method as defined in claim 1, further comprising the step of:

delaying the first timestamp by a first delay amount so as

to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal.

3 (Cancelled). The method as defined in claim 2, further comprising the step of:

delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal.

4 (Currently Amended). The method as defined in claim ~~3~~1, wherein the first delay amount and the second delay amount are substantially equal delay amounts.

5 (Original). The method as defined in claim 1, further comprising the step of:

initializing the difference signal prior to receiving the first timestamp and the second timestamp.

6 (Previously Presented). The method as defined in claim 1, wherein the step of filtering the difference signal comprises filtering the difference signal with a low pass filter such that

the second clock signal is synchronized with the first clock signal based upon the filtered difference signal.

7 (Original). The method as defined in claim 6, further comprising the step of:

initializing the filtered difference signal prior to receiving the first timestamp and the second timestamp.

8 (Previously Presented). The method as defined in claim 1, wherein the step of generating the second clock signal comprises the step of:

controlling the period of a digitally controlled oscillator based upon the filtered difference signal.

9 (Previously Presented). The method as defined in claim 1, wherein the step of generating the second clock signal comprises the step of:

converting the filtered difference signal from a digital difference signal value into an analog difference signal value; and

controlling the period of a voltage controlled oscillator based upon the analog difference signal value.

10 (Original) A computer signal embodied in a carrier wave readable by a computing system and encoding a computer program of instructions for executing a computer process performing the method recited in claim 1.

11 (Currently Amended). An apparatus for synchronizing clocks in a network, the apparatus comprising:

a receiver for receiving a first timestamp and a second timestamp each indicating a respective time instance within the network; and

a phase-locked loop associated with the receiver, the phase-locked loop comprising:

a first delay element for delaying the first timestamp by a first delay amount;

a first differencing element for measuring a first time interval between the first timestamp delayed by the first delay amount and the second timestamp as determined by a first clock signal;

a second delay element for delaying the first timestamp by a second delay amount;

a second differencing element for measuring a second time interval between the first timestamp delayed by the second delay amount and the second timestamp as determined by a second

clock signal;

a third differencing element for generating a difference signal representing a difference between the first time interval and the second time interval;

a filter for filtering the difference signal; and

a variable oscillator for generating the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal.

12 (Cancelled). The apparatus as defined in claim 11, further comprising:

a first delay element for delaying the first timestamp by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal.

13 (Cancelled). The apparatus as defined in claim 12, further comprising:

a second delay element for delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal.

14 (Currently Amended). The apparatus as defined in claim 1~~3~~1, wherein the first delay amount and the second delay amount are substantially equal delay amounts.

15 (Original). The apparatus as defined in claim 11, wherein the second differencing element initializes the difference signal prior to receiving the first timestamp and the second timestamp.

16 (Previously Presented). The apparatus as defined in claim 11, wherein the filter comprises a low pass loop filter for filtering the difference signal such that the second clock signal is synchronized with the first clock signal based upon the filtered difference signal.

17 (Original). The apparatus as defined in claim 16, wherein the loop filter initializes the filtered difference signal prior to receiving the first timestamp and the second timestamp.

18 (Previously Presented). The apparatus as defined in claim 11, wherein the variable oscillator is a digitally controlled oscillator the period of which is controlled based upon the filtered difference signal.

19 (Previously Presented). The apparatus as defined in claim 11, further comprising:

a digital-to-analog converter for converting the filtered difference signal from a digital difference signal value into an analog difference signal value, and wherein the variable oscillator is a voltage controlled oscillator the period of which is controlled based upon the analog difference signal value.

20 (Currently Amended). An article of manufacture for synchronizing clocks in a network, the article of manufacture comprising:

at least one processor readable carrier; and

instructions carried on the at least one carrier;

wherein the instructions are configured to be readable from the at least one carrier by at least one processor and thereby cause the at least one processor to operate so as to:

receive a first timestamp and a second timestamp each indicating a respective time instance within the network;

delay the first timestamp by a first delay amount;

measure a first time interval between the first timestamp delayed by the first delay amount and the second timestamp as determined by a first clock signal;

delay the first timestamp by a second delay amount;

measure a second time interval between the first timestamp delayed by the second delay amount and the second timestamp as determined by a second clock signal;

generate a difference signal representing a difference between the first time interval and the second time interval;

filter the difference signal; and

generate the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal.